REMARKS

Claims 68-78, 80-85 and 107-116 were pending at the time of the 12 January 2006 Final Office Action. Claims 78 and 116 have been cancelled without prejudice, and thus claims 68-77, 80-85 and 107-115 are presently pending in this application. Claims 68-80, 82, 84, 85 and 107 have been amended in this paper.

As a preliminary matter, the undersigned representative and the applicants would like to thank Examiner Leader for holding a personal interview on 5 April 2006. During the personal interview, the previously presented claims were discussed in light of the cited references. The following remarks summarize and expand upon the subject matter discussed during the personal interview, and thus the applicants respectfully request that this paper also constitute the Applicants Interview Summary.

The status of the claims set forth in the Final Office Action dated 12 January 2006 is as follows:

(A) Claims 68-78 and 80-84 were rejected under 35 U.S.C. § 112, second paragraph.

(B) Claims 68-70, 80-85 and 107-115 were rejected under 35 U.S.C. § 103 over the combination of (a) U.S. Patent No. 5,256,274 issued to Poris ("Poris"), (b) Lowenheim, Frederick A., Electroplating, McGraw-Hill, pp. 416-423 ("Lowenheim"), (c) Alkire, Richard, Transient Behavior During Electrodeposition Onto a Metal Strip of High Ohmic Resistance, Journal of Electrochemical Science, Vol. 118, No. 12, pp. 1935-1941 ("Alkire"), (d) U.S. Patent No. 5,685,970 issued to Ameen et al. ("Ameen"), (e) U.S. Patent No. 4,401,521 issued to Ohmura et al. ("Ohmura"), (f) U.S. Patent No. 5,814,557 issued to Venkatraman et al. ("Venkatraman"), and (g) U.S. Patent No. 5,863,666 issued to Merchant et al. ("Merchant").

(C) Claim 116 was rejected under 35 U.S.C. § 103 over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, Venkatraman, Merchant, and U.S. Patent No. 5,256,565 issued to Bernhardt et al. ("Bernhardt").

(D) Claims 68-78 and 80-84 were rejected under 35 U.S.C. § 103 over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, and U.S. Patent No. 6,066,892 issued to Ding et al. ("Ding").

(E) Claims 68-78 and 80-84 were further rejected under 35 U.S.C. § 103 over the combination of Ding, Lowenheim, Alkire, Ameen and Ohmura.

A. Response to Section 112 Rejection

Claims 68-78 and 80-84 were rejected under 35 U.S.C. § 112, second paragraph, on the grounds that these claims did not distinctly claim the subject matter of the invention. More specifically, the Examiner notes that the use of the term "microelectronic workpiece" is not consistent with the use of the term "semiconductor workpiece" in the preamble of independent claims 68, 80, 82 and 84. The Examiner notes a similar issue with the term "microelectronic wafer" in claim 85. Claims 68, 69, 80, 82, 84, 85 and 107 have been amended to delete the term "microelectronic" before each occurrence of "workpiece." The applicants respectfully submit that the claims comply with 35 U.S.C. § 112, second paragraph, and request that this rejection be withdrawn.

B. Response to Section 103 Rejection – Poris, Lowenheim, Alkire, Ameen, Ohmura, Venkatraman and Merchant

Claims 68-78, 80-85 and 107-115 were rejected under 35 U.S.C. § 103 over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, Venkatraman and Merchant. Independent claims 68, 80, 82, 84 and 85 have been amended, and the amendments to these claims include analogous subject matter. The following remarks address the patentability of claim 68 over this combination of references with the understanding that independent claims 80, 82, 84 and 85 are patentable for analogous reasons. The

patentability of claims 80, 82, 84 and 85, however, is not necessarily limited to the reasons discussed below concerning claim 68.

In rejecting previously presented claim 68, the Examiner cites the combination of Poris, Lowenheim, Alkire, Ameen and Ohmura for the proposition that these references teach applying plating power between the surface of the workpiece and an electrode disposed in contact with the plating solution such that the plating power is applied at a first current density for a first period of time and then at a higher second current density for a second period of time. Venkatraman is cited against the claims for the proposition that this reference teaches a process for making an interconnect structure on a semiconductor workpiece that may be formed of copper. Merchant is cited for the proposition that this reference teaches annealing copper to improve a property of the copper. Claim 68 was rejected on the grounds that it would have been obvious to have annealed the workpiece of Poris with an interconnect as taught by Venkatraman using an annealing process as taught by Merchant because a property of the deposited copper would have been improved. The applicants appreciate the Examiner's detailed description of the rejection in the Office Action, but, for the reasons explained below, the applicants respectfully submit that this combination of references fails to disclose or suggest all of the features of amended claim 68.

1. Claim 68 is Directed Toward a Process for Plating Copper Onto a Semiconductor Workpiece Using a Low-Current Initiation Plating Process Followed By an Annealing Process in the Same Tool that Increases the Grain Size of the Copper and Induces Electromigration to Increase the Conductivity of the Copper

Claim 68 is directed toward a process for electrochemical deposition of copper onto a surface of a workpiece in a plating tool. The method comprises providing a workpiece having a dielectric layer in which recesses have been formed, a barrier layer on the dielectric layer, and a copper seed layer on the barrier layer. The surface of the workpiece is exposed to a plating solution in a plating chamber of the tool, and the plating solution includes a principal metals piece comprising copper. The process further includes

applying plating power between the surface of the workpiece and an electrode electrically coupled to the plating solution to electrolytically deposit copper onto the seed layer and into the recesses. The plating power is applied at a first current density for a first period of time to deposit a first amount of the copper into the recesses, and the plating power is subsequently applied at a second current density for a second period of time to deposit a second amount of the copper until the recesses are filled with copper. The second current density is greater than the first current density, and the majority of the copper is deposited onto the surface of the workpiece during the second time period. Additionally, the copper has relatively small grain sizes that fit within the recesses. The method further includes annealing the copper in the recesses at a predetermined elevated temperature after filing the recesses with the copper while the workpiece is within the tool, but before subsequent chemical mechanical polishing processes. The separate annealing procedure increases the grain size of the copper and induces electromigration such that the conductivity of the deposited copper increases.

The method of claim 68 is particularly useful for forming sub-micron interconnects on semiconductor workpieces. At the time of the invention, the industry sought to use copper instead of aluminum for interconnects by depositing copper into trenches and/or holes in a dielectric layer. The present inventors recognized the advantages of initially using a low-current to start a plating process and then using a higher current later in the plating process because this produces a copper deposit with small grain sizes that can fit within small trenches and holes. The inventors, however, also recognized that small grain sizes can impair the electrical performance of pure copper lines. The inventors sought to decouple the process conditions that are necessary for filling very small recesses, namely the low-current initiation process that produces the small grain sizes, from process conditions that produce desirable electrical results. To do this, the inventors determined that a separate annealing procedure performed after depositing the copper into the recesses increases the grain size of the copper and induces electromigration such that the conductivity of the copper increases.

2. The Applied References Teach Annealing Procedures for Doping Non-Copper Layers with Copper or for Enhancing the Ductility of Copper for Flexible Laminates

Venkatraman was cited for the proposition that this reference teaches forming an interconnect structure of copper and annealing the interconnect. Venkatraman, however, is actually directed to using annealing for doping one conductive layer with copper from another conductive layer. Referring to Figures 1 and 2 of Venkatraman, this reference discloses an interconnect structure 10 comprising a barrier layer 13, a first conductive layer 14 that fills the via portion of the interconnect, and a second conductive layer 16 that fills the line portion of the interconnect. (Column 2, lines 33-38.) The first conductive layer 14 is formed by depositing aluminum, copper, or copper alloys using a CVD process. (Column 3, lines 13-24.) The second conductive layer is then formed on the first conductive layer using a PVD process. (Column 3, lines 25-37.) Following the formation of the second conductive layer 16, "an anneal step may be performed *to drive some of the copper* in second conductive layer 16 into the rest of the interconnect structure 10." (Column 3, lines 38-41, emphasis added.) Venkatraman expressly states "the present invention also provides a method for doping an aluminum layer with copper to improve the reliability of the interconnect structure." (Column 4, lines 28-31.) When the teachings of Venkatraman are considered as a whole, it is clear that the annealing step is performed when the second conductive layer 16 contains copper and the first conductive layer 14 is to be doped with copper from the second conductive layer 16. As a result, Venkatraman only teaches the benefit of annealing a bimetallic interconnect to "drive some of the copper in the second conductive layer 16 into the rest of the interconnect structure 10."

Merchant is cited for the proposition that the properties of copper deposits are improved after being annealed at 180°C. Merchant, however, is more specifically directed to improving the fatigue performance of flexible laminates that have a layer of electrodeposited copper foil. Merchant teaches that conventional flexible laminates used in the electronics industry for fabricating flexible connectors, flexible circuit boards and other components are not well suited for applications that require a large number of flex

cycles. To overcome this problem, Merchant teaches forming a flexible laminate having a copper foil on a flexible polymeric material, and annealing the laminate at 180°C to form a copper sheet with grain sizes of about one micron for improving the fatigue performance. (Column 1, lines 55-65.) When the teachings of Merchant are taken as a whole, this reference teaches annealing a flexible device to enhance the flexibility of a copper foil so that the device can be flexed over a large number of cycles.

3. Amended Claim 68 is Not Obvious Over the Combination of References Including Venkatraman and Merchant Because This Combination of References Fails to Disclose or Suggest All the Features of Claim 68

Amended claim 68 is patentable over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, Venkatraman and Merchant because this combination of references fails to disclose or suggest several features of amended claim 68. For example, none of these references discloses electrolytically depositing copper into recesses on a semiconductor wafer. Additionally, these references fail to disclose or suggest a separate annealing procedure that occurs while the workpiece is within the plating tool after plating the copper into the recesses, but before polishing the workpiece in a chemical mechanical polishing process. Furthermore, neither Venkatraman nor Merchant discloses or suggests an annealing process that increases the grain size of the copper and induces electromigration such that the conductivity of the deposited copper increases. The annealing process disclosed in Venkatraman merely teaches doping an interconnect structure with copper from one of two conductive layers of the interconnect structure. The annealing step in Merchant merely teaches heating a copper foil on a flexible laminate to form grain sizes of about one micron to improve the fatigue performance of the copper. It will be appreciated that the large grain sizes disclosed in Merchant are not useful for filling submicron recesses in semiconductor wafers. In light of the foregoing, the cited combination of references fails to disclose or suggest several features of amended claim 68. The applicants respectfully request withdrawal of the rejection of claims 68-77, 80-85 and 107-115 under Section 103 over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura, Venkatraman and Merchant.

Claim 68 is further patentable over this combination of references because there is no suggestion to use the annealing process and structure of Venkatraman with processes that electrolytically deposit copper into recesses on semiconductor workpieces. The claimed combination involves electrolytically depositing copper onto a copper seed layer to form a copper interconnect in a semiconductor workpiece. As a result, heating the claimed copper interconnect would not "drive" copper from one part of the interconnect to another because, except for the barrier layer, the interconnect is already completely copper. Venkatraman's rationale for heating the workpiece to drive copper from one part of the interconnect to another, therefore, is not applicable to the method of amended claim 68. Therefore, a person skilled in the art faced with an electrolytically deposited copper interconnect formed in accordance with claim 68 would not be motivated by Venkatraman or the other prior art to anneal the claimed electrolytically deposited interconnect because it would not achieve the purpose set forth in Venkatraman and it would further reduce the thermal budget of the semiconductor fabrication process.

Claim 68 is still further patentable over this combination of references because there is also no suggestion to use the annealing process of Merchant with processes that electrolytically deposit copper into recesses of semiconductor workpieces. A person skilled in the art also would not combine Merchant with the other references to come up with the features of amended claim 68 because the claimed process is directed toward enhancing the electrical properties of copper interconnects on semiconductor workpieces, but Merchant is directed toward heating a copper foil on a flexible laminate to increase the flexibility of the copper foil. Semiconductor wafers are not flexible, and thus there is no need to increase the flexibility of copper deposits on semiconductor wafers. A person skilled in the art, therefore, would not heat a semiconductor workpiece in a separate annealing process and further reduce the thermal budget of the workpiece to increase the flexibility of copper interconnects. As such, combining Merchant with the cited references to increase the ductility of the deposited copper is based on hindsight reasoning because a person skilled in the art at the time of the invention would not further reduce the thermal

budget of the semiconductor workpiece to increase the flexibility of the electrolytically deposited copper interconnects. Claim 68, therefore, is patentable over combinations of references including Merchant.

C. Response to Section 103 Rejection – Poris, Lowenheim, Alkire, Ameen, Ohmura, Venkatraman, Merchant, and Bernhardt

Claim 116 was rejected under 35 U.S.C. § 103. This claim has been cancelled from the application, and thus this rejection is now moot.

D. Response to Section 103 Rejection – Lowenheim, Alkire, Ameen, Ohmura and Ding

Claims 68-78 and 80-84 were rejected under 35 U.S.C. § 103 over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura and Ding. Ding is cited for the proposition that this references teaches depositing a copper alloy seed layer onto a dielectric layer, depositing relatively pure copper to fill the features, and heating the workpiece after depositing the relatively pure copper. For the reasons explained below, claim 68 is patentable over this combination of references in light of the teachings of Ding.

1. Ding Teaches Annealing the Workpiece to Transform a Copper Alloy Seed Layer into a Barrier Layer

Ding is directed toward a copper metallization structure in which a copper alloy, such as copper-magnesium or copper-aluminum, is deposited over a dielectric layer, and then substantially pure copper is deposited over the copper alloy layer. The copper alloy layer initially serves as a seed layer or a wetting layer for depositing the substantially pure copper layer onto the workpiece. After depositing the pure copper layer onto the seed layer, the workpiece is heated to a sufficiently high temperature to cause the alloying component of the seed layer to migrate to the dielectric layer and form a barrier layer between the copper and the dielectric material. Ding accordingly discloses depositing a copper alloy seed layer directly onto the dielectric layer such that there is no barrier layer until the workpiece is heated.

2. Amended Claim 68 is Patentable Over the Combination of References Including Ding Because This Combination of Reference Fails to Disclose or Suggest All of the Features of Amended Claim 68

Claim 68 is patentable over the combination of Poris, Alkire, Ameen, Ohmura and Ding because this combination of references fails to disclose or suggest several features of amended claim 68. For example, Ding fails to disclose or suggest providing a workpiece with a barrier layer and a seed layer on the barrier layer, and then depositing copper onto the seed layer. Ding, in fact, teaches away from having a seed layer on a barrier layer before electrolytically depositing the bulk copper because the primary inventive aspect of Ding is to form a barrier layer by heating a copper alloy seed layer. Further, this combination of references fails to disclose or suggest annealing the copper to produce larger grain sizes and induce electromigration such that the electrical conductivity of the deposited copper increases. Therefore, amended claim 68 is patentable over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura and Ding.

Amended claim 68 is further patentable over this combination of references because a person skilled in the art would not combine Ding with the other references to heat a copper interconnect formed over a preexisting barrier layer on a semiconductor workpiece. Ding teaches depositing a copper alloy seed layer, filling the feature with copper, and then heating the workpiece to drive the alloying component out of the seed layer such that the alloying component forms a barrier layer between the copper and the dielectric layer. The barrier layer in Ding is formed after forming the seed layer and the copper interconnect. In the claimed method, however, the copper interconnect has a preexisting barrier layer, and thus it follows that there would be no reason to heat the claimed copper interconnect to form a barrier layer as taught by Ding. Moreover, a person skilled in the art would not further reduce the thermal budget of the semiconductor workpiece in the claimed method based on the teachings of Ding because there is no reason to drive any materials out of the claimed copper interconnects as taught by Ding. Therefore, amended claim 68 is further patentable over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura and Ding.

E. Response to Section 104 Rejection – Ding, Lowenheim, Alkire, Ameen and Ohmura

Claims 68-78 and 80-84 were also rejected over the combination of Ding, Lowenheim, Alkire, Ameen and Ohmura. The applicants respectfully submit that this rejection should be withdrawn for the reasons explained above with respect to the rejection of these claims over the combination of Poris, Lowenheim, Alkire, Ameen, Ohmura and Ding.

F. Conclusion

Independent claims 80, 82, 84 and 85 have been amended to include subject matter analogous to the subject matter discussed above with respect to claim 68. Independent claims 80, 82, 84 and 85 are accordingly patentable over the different combinations of references cited in the Final Office Action dated 12 January 2006 for the reasons explained above with respect to claim 68. The dependent claims pending in the application are patentable as depending from one of the independent claims, and also because of the additional features recited in the dependent claims.

In light of the foregoing, all of the pending claims comply with 35 U.S.C. § 112 and are patentable over the cited art. The applicants request reconsideration of the application and respectfully submit that the pending claims are in condition for allowance. If Examiner Leader has any questions or believes a conversation would expedite prosecution of the application, he is encourage to contact the undersigned representative at (206) 359-3258.

Dated: 12 May 2006

Respectfully submitted,

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